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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,900	03/09/2001	Yutaka Takeishi	A286-1	2596

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EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,900	TAKEISHI ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- Th MAILING DATE of this communication appears on the cov r sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims

Claims 1-40, 42-44, 47, and 51-52 have been amended.

Priority

Priority to Japanese Patent Application No. 2000-064532 (March 9, 2000) is claimed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doi (JP-03-116898) in view of Ohno (US 4,646,158) and further in view of Asai et al. (US 6,409159 B1).

Per claims 1-7, 10-17, 20-25, and 28-36: Doi discloses a volume resistor (16)(Applicant's "said device having a variable value and including a value adjustment portion through which said variable value is adjusted") located on a first printed circuit board (12)(Applicant's "signal processing circuit") where the resistor (16) is capable of easy adjustment (PAJ). An insertion hole (17)(Applicant's "a through-hole formed through said signal processing circuit") opposes the resistor (16) so that the resistor (16) can be adjusted (PAJ). The insertion hole (17) must be appropriately dimensioned so that the resistor (16) can conveniently be adjusted, for example, by the application of a screw driver (PAJ). The variable resistor (16) is also in a floating condition as can be seen in Figure 1 of Doi and the insertion hole (17) and resistor (16) are aligned in keeping with the ability to adjust resistance. Furthermore, the printed circuit board and substrate have heights relative to each other as can be seen in Figure 1.

Doi does not appear to explicitly disclose that a mounting member is positioned opposite the through-hole and electrically connects at an edge therefof to the first surface of the signal processing circuit substrate.

Ohno teaches and discloses a liquid crystal television receiver and has, with reference to Figure 4, a variable resistor (225) located on the side of a substrate (229). Specifically, the variable resistor (225) varies voltage applied to the display panel (21) in order to adjust the brightness of the display surface (Column 3, Lines 42-47).

Ohno is evidence that ordinary workers in the field of liquid crystals would have had the reason, suggestion, and motivation to preferentially locate a variable resistor on the side of a

signal processing circuit substrate to easily control voltage applied to a display and to ultimately control brightness.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Doi in view of Ono for a variable resistor positioned opposite the through-hole and electrically connected at an edge therefor to the first surface of the signal processing circuit substrate to easily control voltage applied to a display and to ultimately control brightness.

Doi does not appear to explicitly specify a mounting member (for example, a flexible printed circuit) that connects with the variable resistor.

Asai teaches and discloses a method of supporting a printed circuit board and method of mounting electrical components (Title, entire patent) and wherein electrical circuitry is mounted onto a printed circuit board through a member (e.g., of sponge rubber) that absorbs vibration and shock applied to the board (Summary of the Invention, entire patent) and the printed circuit board is mounted on a side (Id.).

Asai is evidence that ordinary workers in the field of liquid crystals would have had the reason, suggestion, and motivation to support a variable resistor onto a mounting member so that the board could easily absorb shock applied to the board.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Doi in view of Asai to absorb shock as the resistance of the variable resistor is varied.

Per claims 18, 19, 38, and 39: While Doi discloses a volume resistor, the combination of references apply equally to the situation where any electric component, a capacitor or laser trimming resistor, for example, has to be adjusted conveniently and with ease.

Per claims 8, 9, 26, and 27: Doi does not appear to explicitly disclose a plate for reinforcing the printed circuit board that absorbs a compressive force exerted on the board when the variable resistor is adjusted.

Asai teaches a method of supporting a printed circuit board and method of mounting electric components where a member supports the board on a side surface to reduce vibration to the board (Col. 2, Lines 33-35).

Asai is evidence that ordinary workers in the field of liquid crystals would have had the reason, suggestion, and motivation to support a variable resistor onto a mounting member so that the board could easily absorb shock applied to the board.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Doi in view of Asai to reduce vibration to a printed circuit board.

Claims 40-54 rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (US 6,409,159 B1) in view of Doi (JP-03-116898) and further in view of Muramatsu et al. (US 5,703,665).

Per claims 40-54: Asai discloses a method of mounting printed circuit boards (Col. 2, Lines 24-67).

Asai does not appear to explicitly specify a method of adjusting a variable resistor.

Doi discloses a volume resistor (16) located on a first printed circuit board (12) where the resistor is capable of easy adjustment (PAJ). An insertion hole (17) opposes the resistor so that the resistor can be adjusted (PAJ). The insertion hole must be appropriately dimensioned so that the resistor can conveniently be adjusted, for example, by the application of a screw driver (PAJ). The variable resistor is also in a floating condition as can be seen in Figure 1 of Doi and the through hole and resistor are aligned in keeping with the ability to adjust resistance. Furthermore, the printed circuit board and substrate have heights relative to each other as can be seen in Figure 1.

Doi is evidence that ordinary workers in the field of liquid crystals would have had the reason, suggestion, and motivation to adjust a variable resistor to easily control voltage applied to a display device (Abstracts).

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Asai in view of Doi to vary the resistance of a variable resistor so that voltage can applied to a display can be easily controlled.

Asai does not appear to explicitly disclose that the printed circuit board is located on opposite edges of a signal processing circuit substrate.

Muramatsu teaches that a liquid crystal panel has an interposing unit that is located on the vertices of an isosceles triangle (Col. 1, Lines 52-62).

This arrangement protects the liquid crystal display panel from external stresses (Col. 2, Lines 1-3). Thus, even though the liquid crystal panel may be subjected to external stresses, the panel is ultimately protected from damaging forces because of the aforementioned arrangement.

Muramtasu is evened that ordinary workers in the field of liquid crystals would have had the reason, suggestion ,and motivation to locate a printed circuit board located on opposite edges of a signal processing circuit substrate to protect the display from damaging stresses as noted.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Asai in view of Muramatsu for a printed circuit board on opposing edges to minimize stress to a signal processing circuit substrate used in an LCD panel.

Response to Arguments

Applicant's arguments with respect to claims 1-54 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio

Patent Examiner
Art Unit 2871

Robert Kim, SPE

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